REMARKS

The Office Action dated June 16, 2003 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto. Claims 13, 14, and 16-19 are currently pending. Claim 13 is amended. No new matter is presented. In view of the following remarks, Applicants request the favorable consideration of claims 13, 14, and 16-19.

Claim 13 is amended to overcome a typographical error. In the Amendment filed on April 9, 2003, the proper claim amendments were recited in the marked up copy of the claims however, due to a typographical error, the term "serving" was deleted from the clean copy of the claims. Therefore, claim 13 is amended to overcome this typographical error. This amendment is merely cosmetic in nature and does not affect the scope of the invention.

The Office Action rejected claims 13, 14 and 16-19 under 35 U.S.C. §103(a) as being unpatentable over Matsuoka (U.S. Patent 5,640,033) in view of Satoh et al. (U.S. Patent 5,375,069). The Office Action takes the position that Matsuoka and Satoh teach or suggest all the features recited in claims 13, 14 and 16-19. Applicants respectfully disagree.

Claim 13 is directed to a method of manufacturing a semiconductor device for forming a first wiring pattern and second wiring pattern at the same time on a same level. The first wiring pattern is connected to a gate electrode on a gate insulating film formed on a semiconductor region, and the second wiring pattern is connected to the semiconductor region. In patterning of the first and second wiring pattern, a dummy wiring pattern is electrically separated from and placed between the first and second wiring patterns on the same level is left unetched, the dummy wiring pattern not positively serving as any element in a circuit of the semiconductor device.

Claim 16 recites a method of manufacturing a semiconductor device for forming a plurality of first wiring patterns and a second wiring pattern at the same time on a same level. The first wiring patterns each are connected to a gate electrode on a gate insulating film formed on a semiconductor region. The second wiring pattern is connected to the semiconductor region. In patterning the first and second wiring patterns, at least one

dummy wiring pattern, which is electrically separate from and placed between the first and second patterns on the same level is left unetched. The dummy wiring pattern does not positively serve as any element in a circuit of the semiconductor device.

Matsuoka is directed to a semiconductor device having a fine gate structure. Specifically, Matsuoka discloses a method for forming a first wiring layer 51 and a second wiring layer 57. The first wiring layer 51 is electrically connected to a gate electrode 53 via a first contact portion 52. A source region is electrically connected the second wiring layer 57 via a second contact portion 56. A drain region 54b is electrically connected to a third wiring layer via a third contact portion. A third wiring layer 59 is electrically connected to a drain region 55a via a fourth contact portion 60. Thus, Matsouka discloses a first, second and third wiring patterns which are used as a gate, source, and drain electrodes. However, Matsuoka neither teaches nor suggests a dummy wiring pattern as recited in the claimed invention. Specifically, Matsuoka does not teach or suggest a dummy wiring pattern not positively serving as any element in a circuit of the semiconductor device.

Satoh is directed to a wiring processing methods or wiring routes in semiconductor integrated circuits devices. More specifically, Satoh discloses wiring layers that are insulated mutually by inter-level films and wirings that are adjacent to the one another through the inter-level insulating films. The Office Action takes the position that Satoh discloses spaces (23, 24, 25) between the dumpy pattern and the first and second wiring patterns are set generally equal to a minimum pattern space of the first and second wiring layers. (See Column 6, Lines 49-61). However, the wiring layers 14, 15, and 16 are multi-level wiring layers. As such, the wiring layers are on different levels. The wiring layer 16 is connected to the wiring layers 14 and 15. The wiring layer 16 is also connected to a semiconductor element in the substrate 22 through a contact hole 26. As a result, the wiring layer 16 clearly does not serve as a dummy wiring pattern since current is intended to flow through the wiring layer 16. Thus, it is submitted that Sato also fails to teach or suggest the feature of a dummy wiring pattern as recited in the claimed invention. Further, Satoh fails to teach or suggest a dummy wiring pattern. Specifically, Satoh fails to teach or suggest a dummy wiring pattern electrically separated from and placed between the first and second wiring patterns on the same level, is left unetched, and the dummy pattern not positively serving as any element in a circuit of the semiconductor device. Therefore,

Satoh does not cure the deficiencies of Matuoka. As a result, it is submitted that the combination of Matsuoka and Satoh neither teach nor suggest all the features recited in claims 13, 14 and 16-19. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 13 and 16 under 35 U.S.C. 103(a).

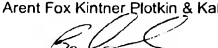
Claims 14, 17, 18 and 19 depend upon claims 13 and 16. Therefore, it is submitted that for at least the reasons mentioned above, claims 14 and 17-19 recite subject matter that is neither taught nor suggested by the applied references. As such, Applicants respectfully request the withdrawal of the rejection of claims 14 and 17-19 under 35 U.S.C. 103(a).

In view of the distinctions discussed above, withdrawal of the rejections to claims 13, 14 and 16-19 is respectfully requested. Claim 13 is amended. No new matter is presented. Accordingly, in view of the above-mentioned distinctions between the claimed invention and the applied references, Applicants submit that the application is now in condition for allowance and that this application be passed to issue.

Should the Examiner believe the application is not in condition for allowance, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicants respectfully petition for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300.

Respectfully submitted,
Arent Fox Kintner Plotkin & Kahn



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